JOINT TECHNOLOGY/CIRCUITS
RUMP SESSION
Wednesday, June 16
8:00 p.m – 10:00 p.m.

Rump Session Organizers:

S. Kosonocky, IBM
M. Nagata, Kobe Univ.
M-R. Lin, AMD
Y. Omura, Kansai Univ.
K. Sakamoto, AIST

RJ1 What's Beyond the Planar MOSFET?
Tapa I
Organizers:

Circuits	**Technology**
K. Bernstein, IBM	M-R. Lin, AMD
K. Mashiko, STARC	Y. Omura, Kansai Univ
	K. Sakamoto, AIST

Moderator: J. Graham, Hewlett Packard
K. Saraswat, Stanford Univ.

The ability to extend the Field Effect Transistor's electrical scaling and on-chip device count beyond the 65 nm lithography node requires reduction in device static leakage currents. Multiple mechanisms now contribute to the overall static power loss. A number of novel non-planar device structure and material remedies have recently been proposed. Each of these approaches, however, introduces new idiosyncrasies and challenges that circuit designers, device/process engineers, and EDA developers would have to accommodate. Our panel of experts on these specific solutions will briefly explain their individual views of the future and the subset of problems their approaches will assert. Our audience of expert technology developers and product designers will have the opportunity to challenge their conclusions and judge which of the scenarios is most likely to resemble the future direction for our industry.

Panelists

G. Bernstein, Norte Dame Univ.
R. Chau, Intel
Y. Hagiwara, Sony
Y. Nishi, Stanford
L. Scheffer, Cadence
H-S P. Wong, IBM
K. Yano, Hitachi